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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,215	11/19/2003	Kenneth Stern	A2WI2320US	9062

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EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,215	STERN, KENNETH	
	Examiner	Art Unit	
	John H. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *13-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7 and 11* is/are rejected.

7)☒ Claim(s) *4-6,8-10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/19/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I (Claims 1-12) in Paper mailed on 03/07/2005 with without traverse is acknowledged. Accordingly, claims 13-25 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03. Applicant has the right to file a divisional application covering the subject matter of the non-elected claims 13-25.

2. Claims 13-25 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper mailed on 03/07/2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 3, 7, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Stern (USP 6,242,959).

Regarding claim 1, Stern discloses a method of autocalibrating a plurality of phase delayed clock signal edges within a reference clock period (e.g. Fig.1, Col.1, lines 55-64), comprising: measuring delay spacings between said plurality of clock signal edges (Col.1, lines 40-44, Col.8, lines 25-27); calculating desired

delay spacings from said delay spacings (e.g. Col.2, lines 62-67); calculating ideal signal edges from said desired delay spacings (Col.3, lines 63-68); and adjusting (fixed delay) said clock signal edges to match said respective ideal signal edges (leading edge of the a desired clock pulse)(e.g. Col.6, lines 6-23); wherein said plurality of clock signal edges are selectively available (Col.4, lines 19-21).

Regarding claim 2, Stern discloses measuring a wrap-around delay spacing between the last and first signal edges of said plurality of clock signal edges to reduce error in said calculation of desired delay spacing (e.g. Fig.4, Col.6, lines 6-13).

Regarding claim 3, Stern discloses said desired delay spacings are calculated by: calculating an average delay spacing so that the calibrated clock signal edges form an approximately linear time reference (e.g. Col.5, lines 47-53).

Regarding claim 7, Stern discloses delay spacings are measured by: delaying a first clock signal edge of said plurality of clock signal edges to determine said delay spacing (e.g. Col.1, lines 43-47).

Regarding claim 11, Stern discloses calculating error delays between said clock signal edges and respective next ideal signal edges to enable said adjusting of said clock signals based on said calculated error delays (e.g. Col.4, line 60-Col.5, line 3, Col.6, lines 6-13).

Allowable Subject Matter

5. Claims 4-6, 8-10, and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 4, none of the prior art of record teaches or suggests the combination of a method of autocalibrating a plurality of phase delayed clock signal edges within a reference clock period, wherein the method comprising steps of: measuring delay spacings between said plurality of clock signal edges; calculating desired delay spacings from said delay spacings; calculating ideal signal edges from said desired delay spacings; and adjusting said clock signal edges to match said respective ideal signal edges; wherein said plurality of clock signal edges are selectively available; wherein, for each successive pair of clock signal edges in said plurality of clock signal edge, said delay spacings are measured by: comparing the first and second clock signal edges to determine which arrives first. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 5, none of the prior art of record teaches or suggests the combination of a method of autocalibrating a plurality of phase delayed clock signal edges within a reference clock period, wherein the method comprising steps of: measuring delay spacings between said plurality of clock signal edges; calculating desired delay spacings from said delay spacings; calculating ideal

signal edges from said desired delay spacings; and adjusting said clock signal edges to match said respective ideal signal edges; wherein said plurality of clock signal edges are selectively available; wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by: switching first and second clock signal edges of said plurality of clock signal edges to target and delay signal paths, respectively; and comparing the phases of said first and second clock signal edges. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 6, none of the prior art of record teaches or suggests the combination of a method of autocalibrating a plurality of phase delayed clock signal edges within a reference clock period, wherein the method comprising steps of: measuring delay spacings between said plurality of clock signal edges; calculating desired delay spacings from said delay spacings; calculating ideal signal edges from said desired delay spacings; and adjusting said clock signal edges to match said respective ideal signal edges; wherein said plurality of clock signal edges are selectively available; wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by: delaying a first clock signal edge of said plurality of clock signal edges by one period with a one period delay circuit; and comparing the phases of said first clock signal edge to the phase of a second clock signal edge of said plurality of clock signal edges. It is these limitations as they are claimed in the

combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 8, none of the prior art of record teaches or suggests the combination of a method of autocalibrating a plurality of phase delayed clock signal edges within a reference clock period, wherein the method comprising steps of: measuring delay spacings between said plurality of clock signal edges; calculating desired delay spacings from said delay spacings; calculating ideal signal edges from said desired delay spacings; and adjusting said clock signal edges to match said respective ideal signal edges; wherein said plurality of clock signal edges are selectively available; wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by: adjusting a first clock signal to match a second clock signal edge, each of said first and second clock signals of said plurality of clock signal edges; and determining said delay spacings from said adjustment. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 9, none of the prior art of record teaches or suggests the combination of a method of autocalibrating a plurality of phase delayed clock signal edges within a reference clock period, wherein the method comprising steps of: measuring delay spacings between said plurality of clock signal edges; calculating desired delay spacings from said delay spacings; calculating ideal

signal edges from said desired delay spacings; and adjusting said clock signal edges to match said respective ideal signal edges; wherein said plurality of clock signal edges are selectively available; wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by: incrementing a calibration control register to induce a change in delay of a first clock edge to match a delay of a second clock edge, said first and second clock edges of said plurality of clock signal edges; and taking the resulting value of the calibration control register as the delay spacing measurement. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 10, none of the prior art of record teaches or suggests the combination of a method of autocalibrating a plurality of phase delayed clock signal edges within a reference clock period, wherein the method comprising steps of: measuring delay spacings between said plurality of clock signal edges; calculating desired delay spacings from said delay spacings; calculating ideal signal edges from said desired delay spacings; and adjusting said clock signal edges to match said respective ideal signal edges; wherein said plurality of clock signal edges are selectively available; wherein, for each successive pair of clock signal edges in said plurality of clock signal edges, said delay spacings are measured by: decrementing a calibration control register to induce a change in delay of a first clock edge to match a delay of a second clock edge, said first and second clock edges of said plurality of clock signal edges; and taking the

resulting value of the calibration control register as the delay spacing. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 12, none of the prior art of record teaches or suggests the combination of a method of autocalibrating a plurality of phase delayed clock signal edges within a reference clock period, wherein the method comprising steps of: measuring delay spacings between said plurality of clock signal edges; calculating desired delay spacings from said delay spacings; calculating ideal signal edges from said desired delay spacings; adjusting said clock signal edges to match said respective ideal signal edges; wherein said plurality of clock signal edges are selectively available; calculating error delays between said clock signal edges and respective next ideal signal edges to enable said adjusting of said clock signals based on said calculated error delays; and saving said error delays for subsequent retrieval. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Other Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Miller (USP 5,488,369) disclose a sampling apparatus comprising a clock signal generator, a plurality of devices each driven by a respective clock signal

from said generator whereby to time multiplex said devices, variable delay means for selectively delaying the respective clock signals from the generator, means for supplying a reference timing signals to said devices, and means for adjusting the variable delay means in response to the application of said two signals whereby to calibrate said plurality of devices.

Kim et al. (USP 6,396,322) disclose a delay locked loop for use in a semiconductor memory device.

Orihashi et al. (USP 5438259) disclose a digital circuitry apparatus in which clock distribution can be performed with high accuracy even in the case where variations in delay time are caused by variations in the apparatus operating condition, programmed input data set to delay circuits are corrected by a circuit portion for measuring the delay time of a phase shifting adjustment delay circuit with respect to variations in delay time caused by variations in the apparatus operating condition

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MICHAEL NGHIEM
PRIMARY EXAMINER

John H. Le

Patent Examiner-Group 2863

April 8, 2005